

Remarks

Claims 1 and 2 are pending in the subject application and currently stand rejected. Reconsideration and favorable consideration of the pending claims is respectfully requested in view of the following remarks.

Claims 1 and 2 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu *et al.* (U.S. 6,913,980) in view of Kakimoto *et al.* (U.S. 5,166,087). Applicant respectfully traverses. Wu, alone or in combination with Kakimoto, fails to teach or suggest a method for fabricating a transistor comprising removing the nitride layer and the first oxide layer on the surface of the substrate such that the nitride layer and the first oxide layer remain on the substrate only below the spacers after forming the second preliminary source/drain region through the second ion implantation process using the spacers as a mask as specified in subject claim 1. Rather, Wu teaches removing the nitride layer **330** and the first oxide layer **328** before forming the source and drain regions **342, 344** through implanting the dopants **340** (*see* Figs. 19-21 of Wu).

In addition, it appears that the Office Action, at page 3, indicates that Figure 23 of Wu shows a step subsequent to the implant step shown in Figure 21. That is, the Action at pages 2-3, states that Wu teaches a method comprising:

“forming spacers on sidewalls **334/336** of the gate electrode, forming a second preliminary source/drain region **344** through a second ion implantation process using the spacers as a mask (figure 21), removing the nitride layer and the first oxide layer on the surface of the substrate such that the nitride layer and the first oxide layer remain on the substrate only below the spacers after forming the second preliminary source/drain region through the second ion implantation process using the spacers as a mask (figure 23)”

However, Figure 23 does not show a subsequent step to the process shown in Figure 21. Rather, Figure 23 shows an alternative embodiment for comparison of the separation between the deep compensation implants **380, 350** where the spacers **334, 336** are not selectively etched/processed (*see* col. 11, lines 10-35). In particular, Figure 20 (and Figures 21-22) shows the spacer being etched/ processed after performing a step shown in Figure 19, and Figure 23 shows a result of performing the steps of Figures 20-22 without the spacer being etched/ processed. Specifically, Figure 19 shows a nitride layer **330** being removed before forming the source and drain regions (*see* col. 9, lines 56-58). Then, Figure 20 shows a subsequent process to that of Figure 19,

where the remaining oxide layer is removed (*see* col. 10, lines 8-11). The step shown in Figure 21 is subsequent to the step of Figure 20, and shows the formation of the source and drain regions (*see* col. 10, lines 34-35). Figure 23 shows an alternative embodiment having the oxide layer 328 removed and source/drain region formed, but where the sidewall spacers have not been processed as with the steps shown in Figure 20. Thus, Figure 23 does not show a subsequent step to the process shown in Figure 21.

Furthermore, based on either embodiment, Wu fails to teach or suggest removing the nitride layer and the first oxide layer after forming the second preliminary source/drain region.

Kakimoto fails to cure these deficiencies. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

In view of the foregoing remarks, Applicant believes that the claims as currently pending are in condition for allowance, and such action is respectfully requested.

Applicant invites the Examiner to call the undersigned if clarification is needed on any of this response, or if the Examiner believes a telephonic interview would expedite the prosecution of the subject application to completion.

The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 or 1.17 as required by this paper to Deposit Account 19-0065.

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